

Dual N-Channel Enhancement Mode MOSFET

Features

- Surface-mounted package
- Extremely low threshold voltage
- Advanced trench cell design
- ESD protected (HBM>2KV)

Applications

- Portable appliances
- Battery management

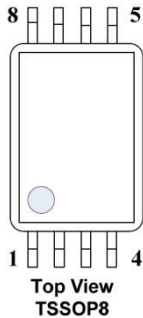
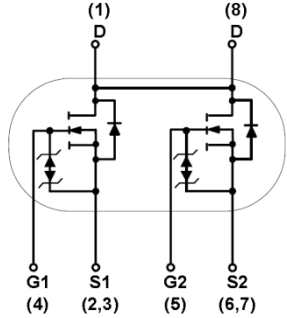
Quick reference

- $BV \cong 20\text{ V}$ $P_{tot} \cong 1.25\text{ W}$ $I_D \cong 6.8\text{ A}$
- $R_{DS(ON)} \cong 18\text{ m}\Omega @ V_{GS} = 4.5\text{ V}$ / $R_{DS(ON)} \cong 27\text{ m}\Omega @ V_{GS} = 2.5\text{ V}$

TSSOP8



Pin Description

Pin Description	Simplified Outline	Symbol
1 Drain(D) 2,3 Source(S1) 4 Gate(G1) 5 Gate(G2) 6,7 Source(S2) 8 Drain(D)	 <p>Top View TSSOP8</p>	

Limiting Values

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	Drain-Source Voltage	$T_A = 25\text{ }^\circ\text{C}$	-	20	V
V_{GS}	Gate-Source Voltage	$T_A = 25\text{ }^\circ\text{C}$	-	± 12	V
I_D^*	Drain Current	$T_A = 25\text{ }^\circ\text{C}, V_{GS} = 4.5\text{ V}$	-	6.8	A
		$T_A = 100\text{ }^\circ\text{C}, V_{GS} = 4.5\text{ V}$	-	4.3	A
I_{DM}^{***}	Pulsed Drain Current	$T_A = 25\text{ }^\circ\text{C}, V_{GS} = 4.5\text{ V}$	-	24	A
P_{tot}	Total Power Dissipation	$T_A = 25\text{ }^\circ\text{C}$	-	1.25	W
T_{stg}	Storage Temperature		-55	150	$^\circ\text{C}$
T_J	Junction Temperature		-55	150	$^\circ\text{C}$
I_S	Diode Forward Current	$T_A = 25\text{ }^\circ\text{C}$	-	1.5	A
$R_{\theta JA}^*$	Thermal Resistance- Junction to Ambient			100	$^\circ\text{C} / \text{W}$

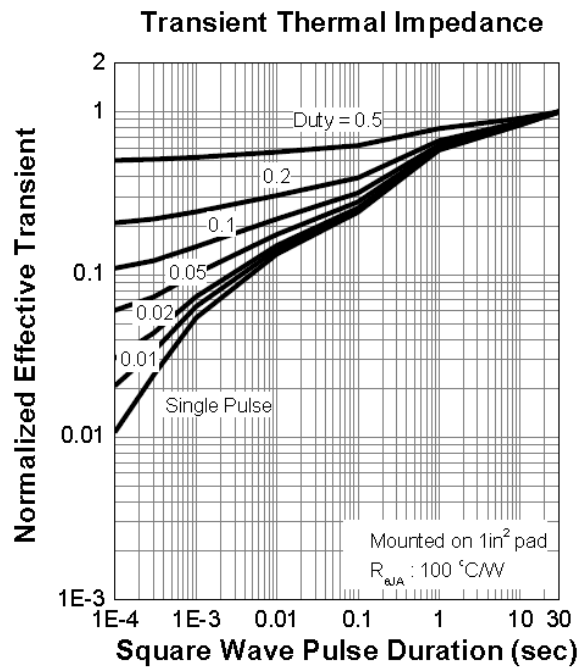
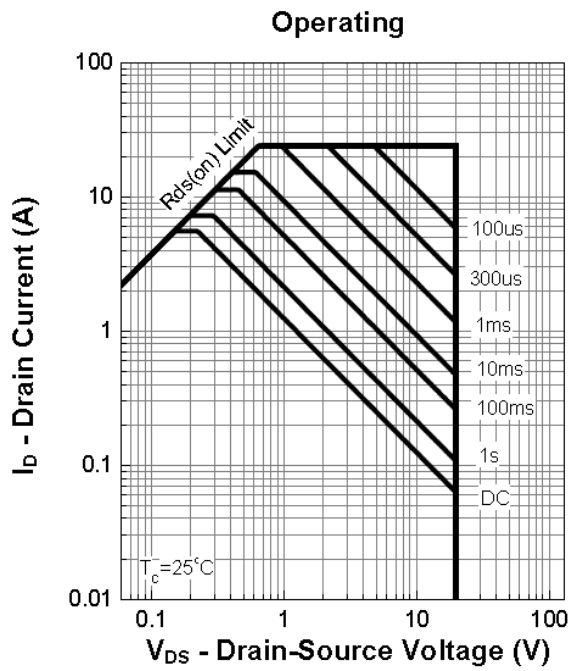
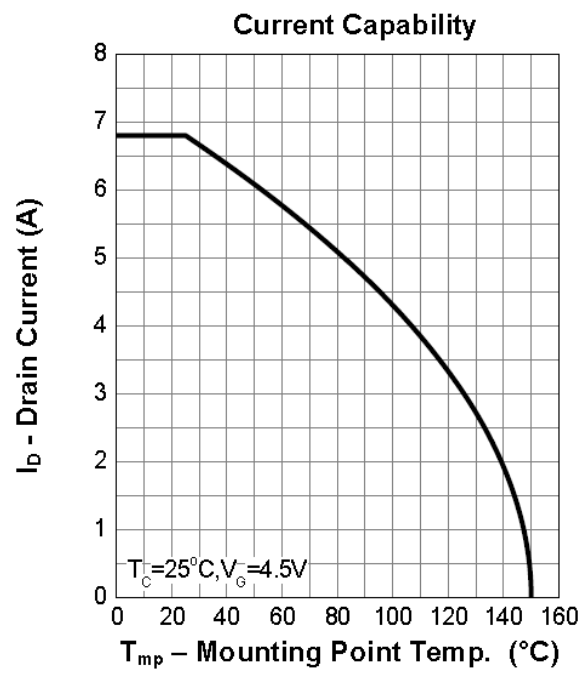
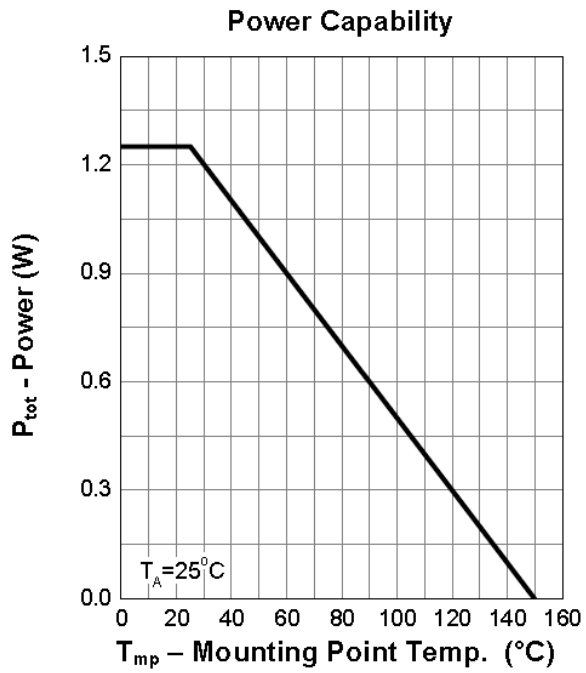
Notes : * Surface Mounted on 1 in² pad area, t ≤ 10 sec ** Pulse width ≤ 300 μs, duty cycle ≤ 2 %

Electrical Characteristics (TA = 25 °C Unless Otherwise Noted)

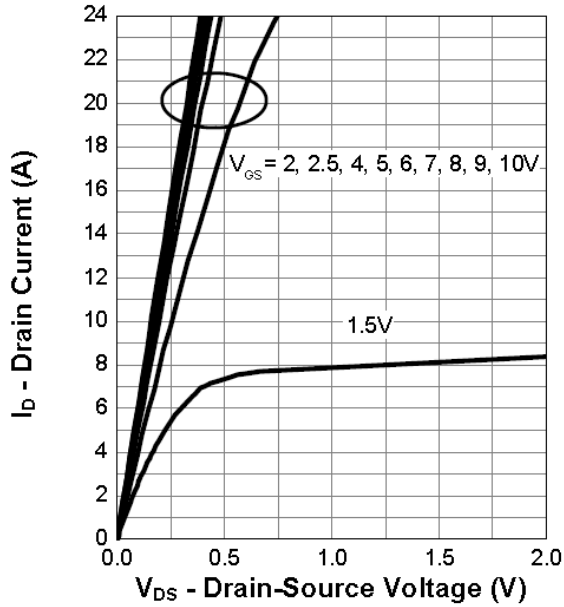
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_{DS} = 250\ \mu\text{A}$	20	-	-	V
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_{DS} = 250\ \mu\text{A}$	0.5	0.7	1	V
I_{DSS}	Drain Leakage Current	$V_{DS} = 16\text{ V}, V_{GS} = 0\text{ V}$	-	-	1	μA
		$T_J = 85\text{ }^\circ\text{C}$	-	-	30	μA
I_{GSS}	Gate Leakage Current	$V_{GS} = \pm 10\text{ V}, V_{DS} = 0\text{ V}$	-	-	± 10	μA
		$V_{GS} = \pm 4.5\text{ V}, V_{DS} = 0\text{ V}$	-	-	± 0.8	
$R_{DS(ON)}^a$	On-State Resistance	$V_{GS} = 4.5\text{ V}, I_{DS} = 6.8\text{ A}$	-	14	18	m Ω
		$V_{GS} = 2.5\text{ V}, I_{DS} = 5\text{ A}$	-	19	27	
Diode Characteristics						
V_{SD}^a	Diode Forward Voltage	$I_{SD} = 1.5\text{ A}, V_{GS} = 0\text{ V}$	-	0.7	1.1	V
t_r	Reverse Recovery Time	$I_{SD} = 6.8\text{ A}, dI_{SD}/dt = 100\text{ A}/\mu\text{s}$	-	29	-	ns
Q_{rr}	Reverse Recovery Charge		-	16	-	nC
Dynamic Characteristics^b						
R_G	Gate Resistance	$V_{GS} = V_{DS} = 0\text{ V}, F = 1\text{ MHz}$	-	4	-	Ω
C_{iss}	Input Capacitance	$V_{GS} = 0\text{ V}, V_{DS} = 10\text{ V}$ Frequency = 1 MHz	-	850	-	pF
C_{oss}	Output Capacitance		-	200	-	
C_{rss}	Reverse Transfer Capacitance		-	185	-	
$t_{d(on)}$	Turn-on Delay Time	$V_{DS} = 10\text{ V}, V_{GEN} = 4.5\text{ V},$ $R_G = 6\ \Omega, R_L = 10\ \Omega,$ $I_{DS} = 1\text{ A}$	-	7	12	ns
t_r	Turn-on Rise Time		-	11	24	
$t_{d(off)}$	Turn-off Delay Time		-	63	120	
t_f	Turn-off Fall Time		-	38	65	
Gate Charge Characteristics^b						
Q_g	Total Gate Charge	$V_{GS} = 4.5\text{ V}, V_{DS} = 10\text{ V},$ $I_{DS} = 6.8\text{ A}$	-	18.5	-	nC
Q_{gs}	Gate-Source Charge		-	1.2	-	
Q_{gd}	Gate-Drain Charge		-	7.4	-	

Notes : a : Pulse test ; pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$ b : Guaranteed by design, not subject to production testing

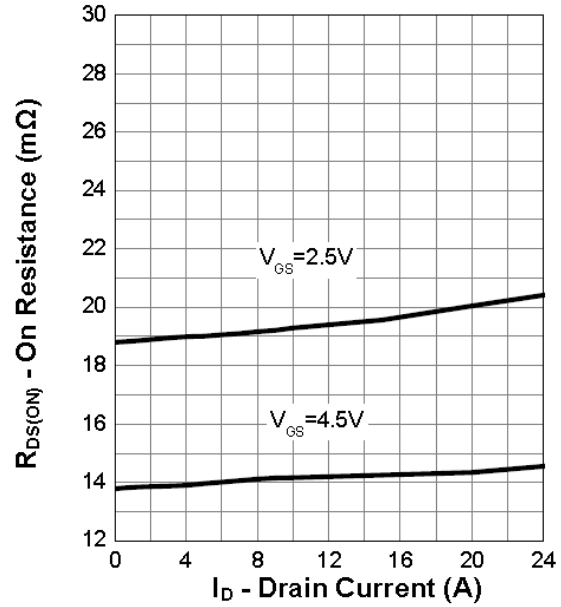
Typical Characteristics



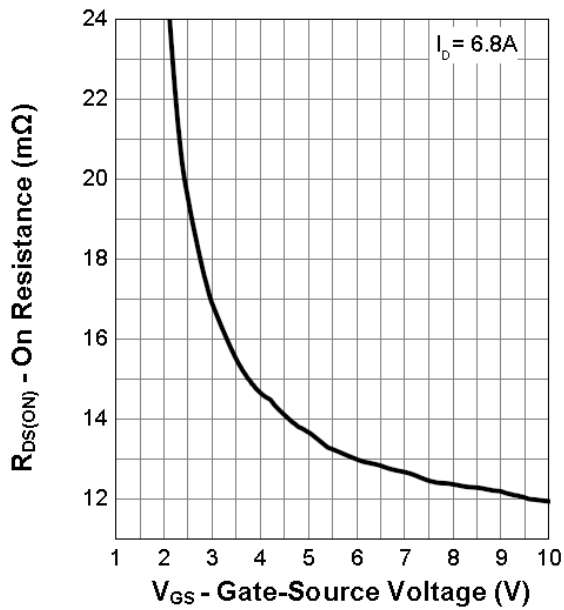
Output Characteristics



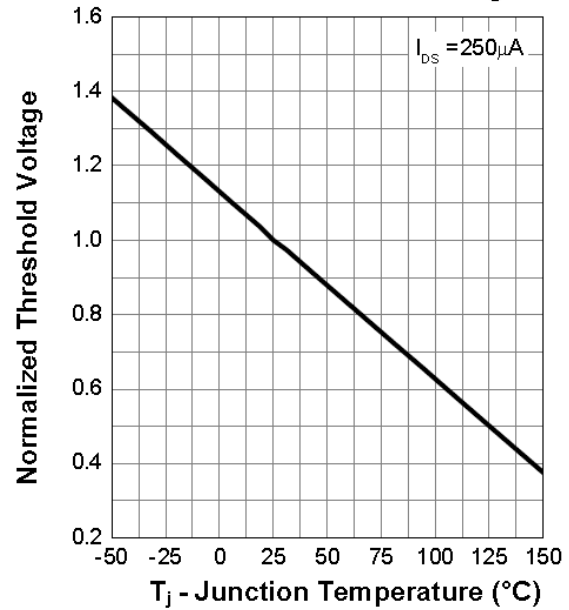
On Resistance

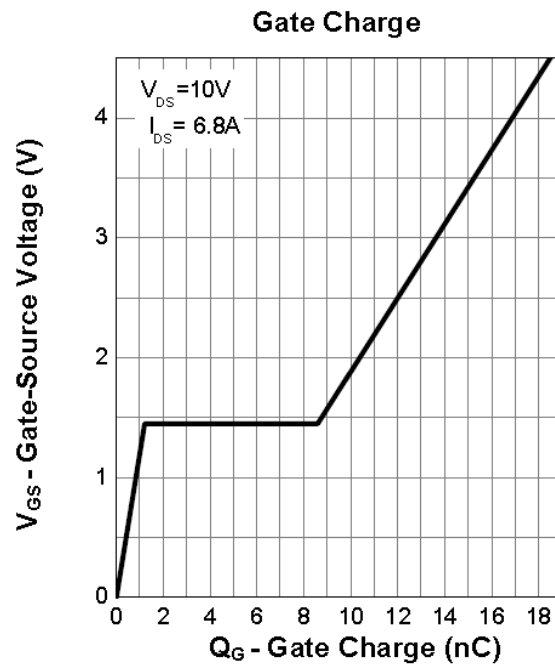
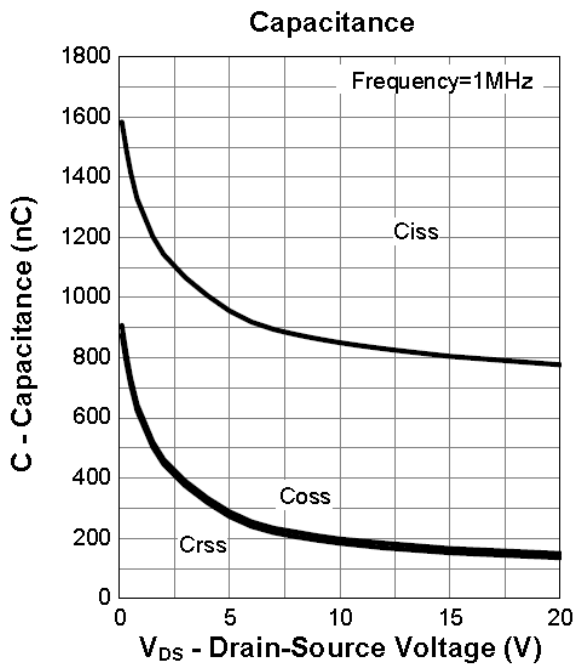
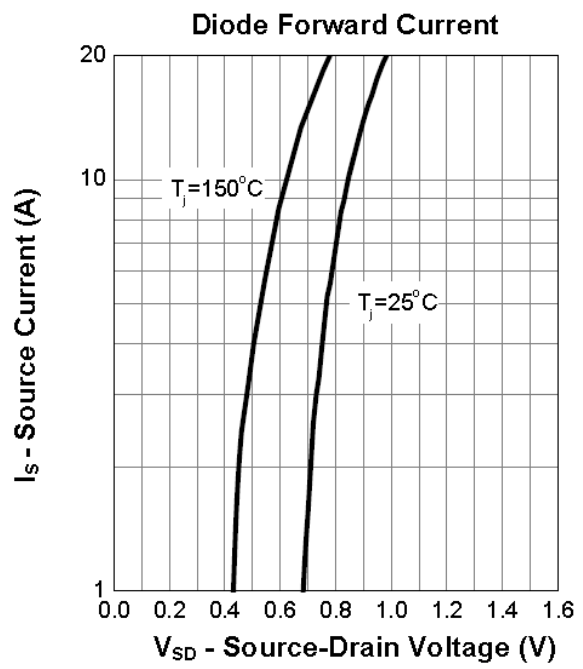
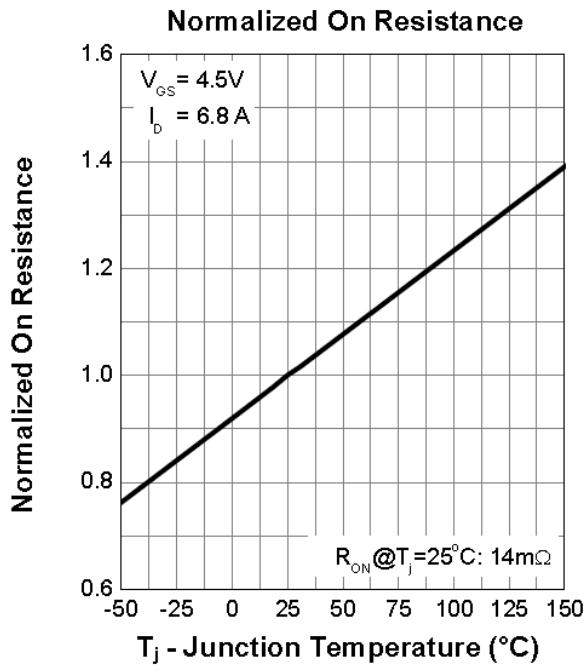


Transfer Characteristics



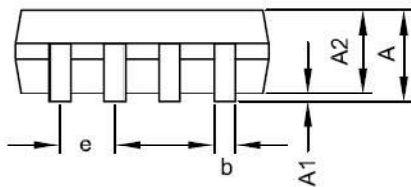
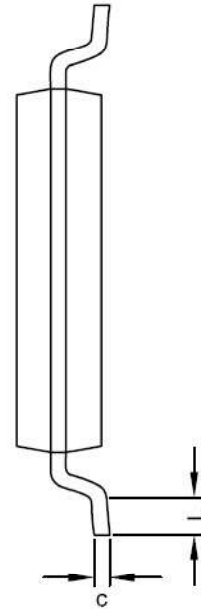
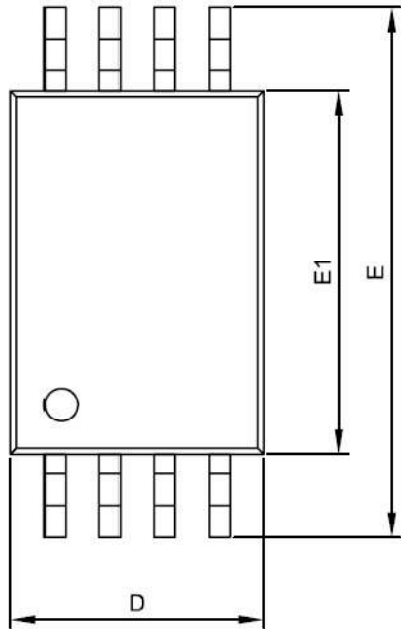
Normalized Threshold Voltage





Package Dimensions

TSSOP-8



Symbol	Dimensions In Millimeters	
	MIN.	MAX.
A	—	1.20
A1	0.00	0.15
A2	0.85	1.05
D	2.90	3.10
E	6.20	6.60
E1	4.30	4.50
c	0.09	0.20
b	0.19	0.30
e	0.65 BSC	
L	0.45	0.75