

N-Channel Enhancement Mode Field Effect Transistor

Product Summary

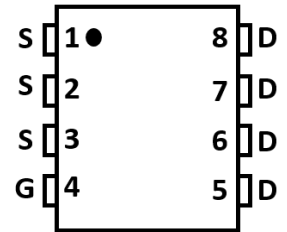
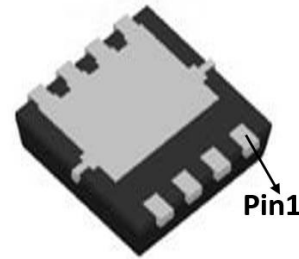
- V_{DS} 30V
- I_D 50A
- $R_{DS(ON)}$ (at $V_{GS}=10V$) <6.0 mohm
- $R_{DS(ON)}$ (at $V_{GS}=4.5V$) <8.0 mohm
- 100% UIS Tested
- 100% ∇V_{DS} Tested

General Description

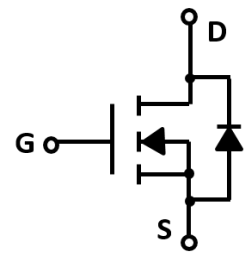
- Trench Power LV MOSFET technology
- Excellent package for heat dissipation
- High density cell design for low $R_{DS(ON)}$

Applications

- High current load applications
- Load switching
- Hard switched and high frequency circuits
- Uninterruptible power supply
- **Marking** : Q50N03B



DFN3.3X3.3



Absolute Maximum Ratings ($T_A=25^\circ\text{C}$ unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-source Voltage		V_{DS}	30	V
Gate-source Voltage		V_{GS}	± 20	V
Drain Current	$T_C=25^\circ\text{C}$	I_D	50	A
	$T_C=100^\circ\text{C}$		35	
Pulsed Drain Current ^A		I_{DM}	190	A
Total Power Dissipation	$T_C=25^\circ\text{C}$	P_D	30	W
	$T_C=100^\circ\text{C}$		15	W
Single Pulse Avalanche Energy ^B		E_{AS}	225	mJ
Thermal Resistance Junction-to-Case ^C		$R_{\theta JC}$	5	$^\circ\text{C}/\text{W}$
Junction and Storage Temperature Range		T_J, T_{STG}	-55~+175	$^\circ\text{C}$

Electrical Characteristics (T_J=25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} = 0V, I _D =250μA	30			V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =30V, V _{GS} =0V			1	μA
Gate-Body Leakage Current	I _{GSS}	V _{GS} = ±20V, V _{DS} =0V			±100	nA
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D =250μA	1.0	1.5	2.5	V
Static Drain-Source On-Resistance	R _{DS(ON)}	V _{GS} = 10V, I _D =15A		4.9	6.0	mΩ
		V _{GS} = 4.5V, I _D =15A		6.3	8.0	
Diode Forward Voltage	V _{SD}	I _S =20A, V _{GS} =0V			1.2	V
Maximum Body-Diode Continuous Current	I _S				50	A
Dynamic Parameters						
Input Capacitance	C _{iss}	V _{DS} =15V, V _{GS} =0V, f=1MHZ		2150		pF
Output Capacitance	C _{oss}			435		
Reverse Transfer Capacitance	C _{rss}			252		
Switching Parameters						
Total Gate Charge	Q _g	V _{GS} =10V, V _{DS} =15V, I _D =20A		52.8		nC
Gate-Source Charge	Q _{gs}			12.3		
Gate-Drain Charge	Q _{gd}			10.8		
Reverse Recovery Charge	Q _{rr}	I _F =25A, di/dt=100A/us		28		
Reverse Recovery Time	t _{rr}			27		
Turn-on Delay Time	t _{D(on)}	V _{GS} =10V, V _{DD} =20V, I _D =4A, R _L =1Ω R _{GEN} =3Ω		9		ns
Turn-on Rise Time	t _r			15.5		
Turn-off Delay Time	t _{D(off)}			29		
Turn-off fall Time	t _f			9		

A. Pulse Test: Pulse Width ≤ 300us, Duty cycle ≤ 2%.

B. T_J=25°C, V_{DS}=30V V_{DD}=25V V_{GS}=10V L=1mH.

C. R_{θJA} is the sum of the junction-to-case and case-to-ambient thermal resistance, where the case thermal reference is defined as the solder mounting surface of the drain pins. R_{θJC} is guaranteed by design, while R_{θJA} is determined by the board design. The maximum rating presented here is based on mounting on a 1 in 2 pad of 2oz copper.

Typical Performance Characteristics

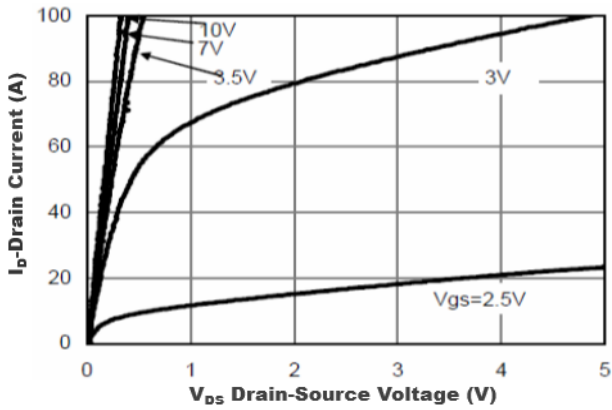


Figure1. Output Characteristics

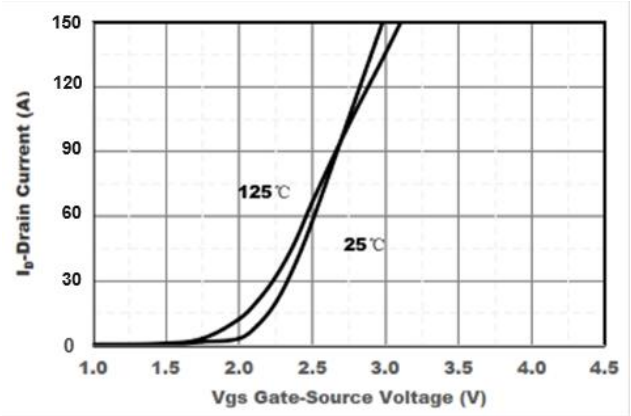


Figure2. Transfer Characteristics

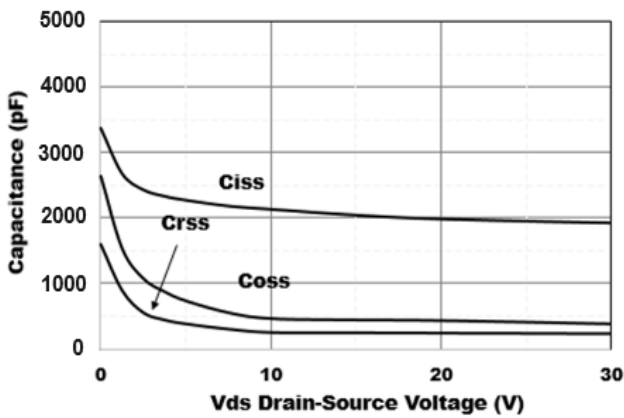


Figure3. Capacitance Characteristics

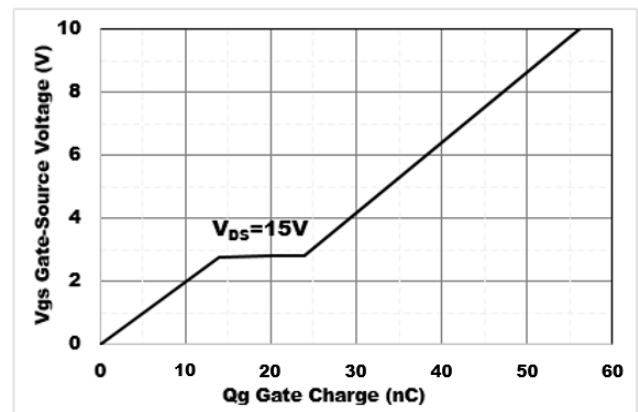


Figure4. Gate Charge

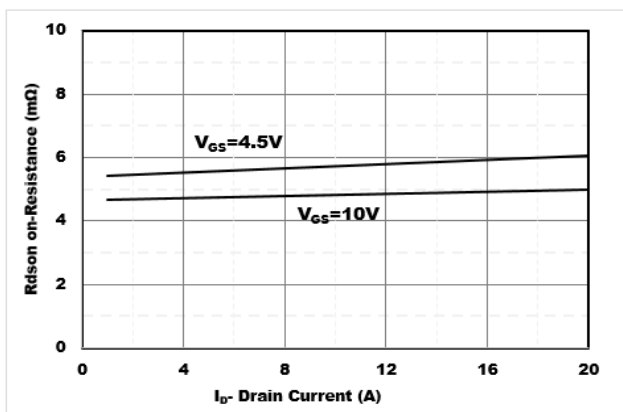


Figure5. Drain-Source on Resistance

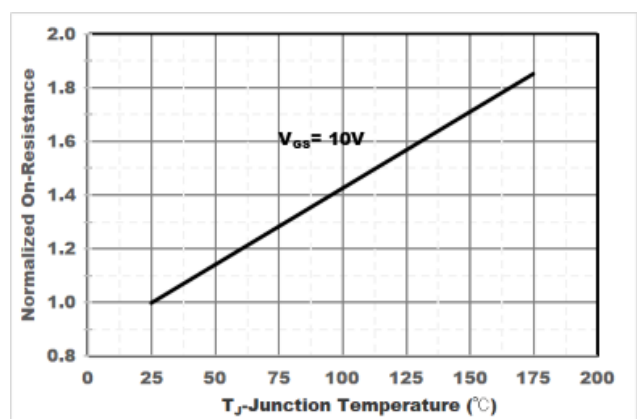


Figure6. Drain-Source on Resistance

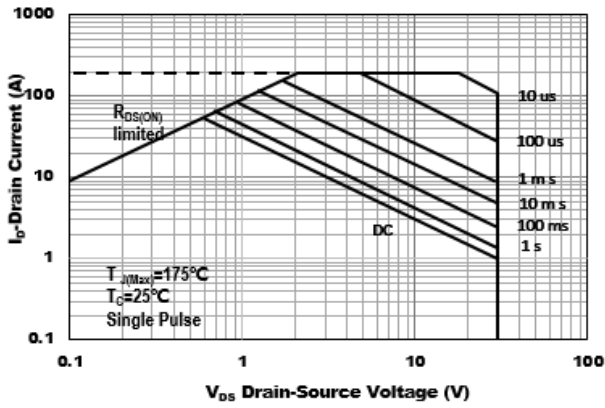


Figure7. Safe Operation Area

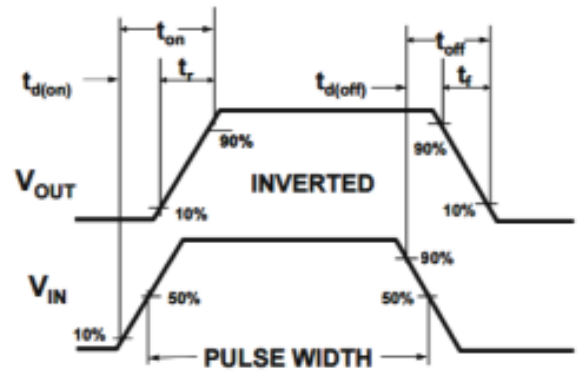
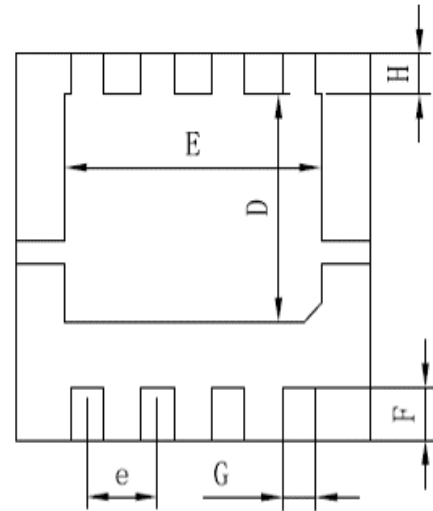
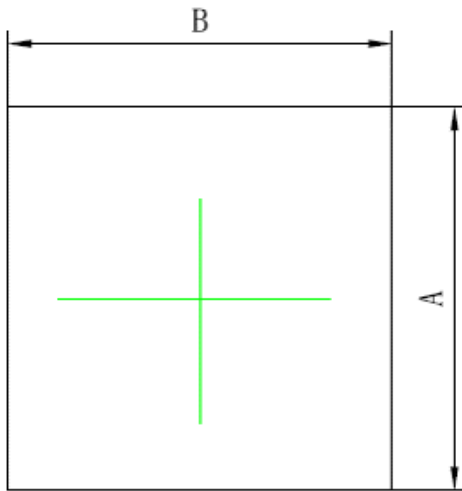


Figure8. Switching wave

DFN3.3X3.3 Package information



A	B	C	C1
3.25±0.05	3.25±0.05	0.8±0.05	0.2±0.02
C2	D	E	F
0.05Max	1.9±0.1	2.35±0.15	0.45±0.05
G	H	e	
0.3±0.05	0.35±0.05	0.65±0.05	
: mm			

