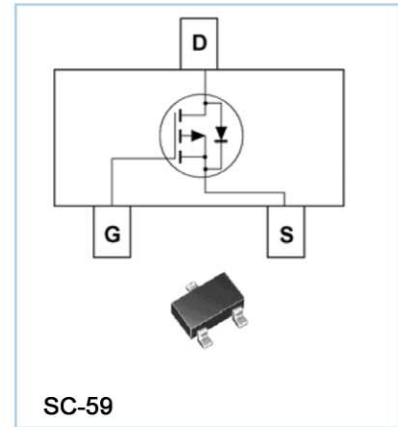


P-Channel Enhancement Mode MOSFET

Feature

- -16V/-4A, $R_{DS(ON)} = 90\text{m}\Omega$ (MAX) @ $V_{GS} = -4.5\text{V}$.
 $R_{DS(ON)} = 130\text{m}\Omega$ (MAX) @ $V_{GS} = -2.5\text{V}$.
- Super High dense cell design for extremely low $R_{DS(ON)}$
- Reliable and Rugged
- SC-59 for Surface Mount Package



Applications

- Power Management
Portable Equipment and Battery Powered Systems.

Absolute Maximum Ratings

$T_A = 25^\circ\text{C}$ Unless Otherwise noted

Parameter	Symbol	Limit	Units
Drain-Source Voltage	V_{DS}	-16	V
Gate-Source Voltage	V_{GS}	± 8	V
Drain Current-Continuous	I_D	-4	A

Electrical Characteristics

$T_A = 25^\circ\text{C}$ Unless Otherwise noted

Parameter	Symbol	Test Conditions	Min	Typ.	Max	Units
Off Characteristics						
Drain to Source Breakdown Voltage	BVDSS	$V_{GS} = 0\text{V}, I_D = -250\mu\text{A}$	-16	-	-	V
Zero-Gate Voltage Drain Current	IDSS	$V_{DS} = -12\text{V}, V_{GS} = 0\text{V}$	-	-	-1	μA
Gate Body Leakage Current, Forward	IGSSF	$V_{GS} = 8\text{V}, V_{DS} = 0\text{V}$	-	-	100	nA
Gate Body Leakage Current, Reverse	IGSSR	$V_{GS} = -8\text{V}, V_{DS} = 0\text{V}$	-	-	-100	nA
On Characteristics						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{GS} = V_{DS}, I_D = -250\mu\text{A}$	-0.5	-	-1.5	V
Static Drain-source On-Resistance	$R_{DS(ON)}$	$V_{GS} = -4.5\text{V}, I_D = -4.0\text{A}$	-	-	90	$\text{m}\Omega$
		$V_{GS} = -2.5\text{V}, I_D = -2.0\text{A}$	-	-	130	$\text{m}\Omega$
Drain-Source Diode Characteristics and Maximum Ratings						
Drain-Source Diode Forward Voltage	VSD	$V_{GS} = 0\text{V}, I_S = -1.25\text{A}$			-1.2	V

Typical Characteristics

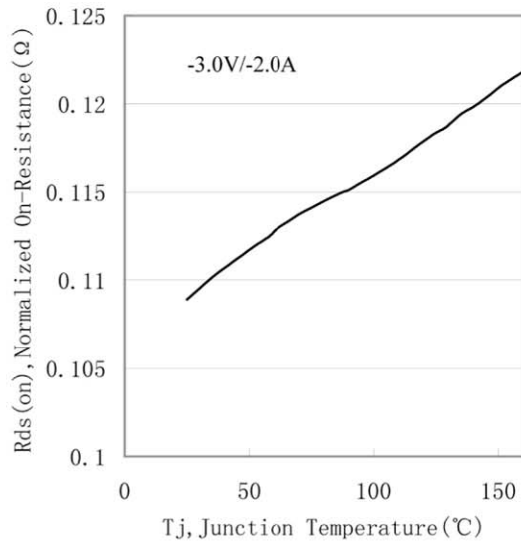


Figure 5. On-Resistance Variation with Temperature

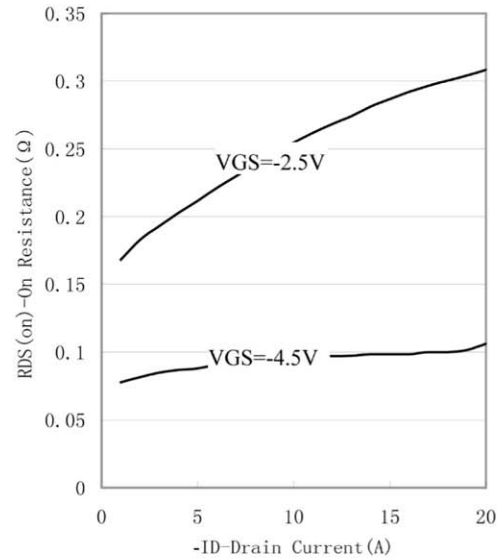


Figure 6. On-Resistance vs. Drain Current

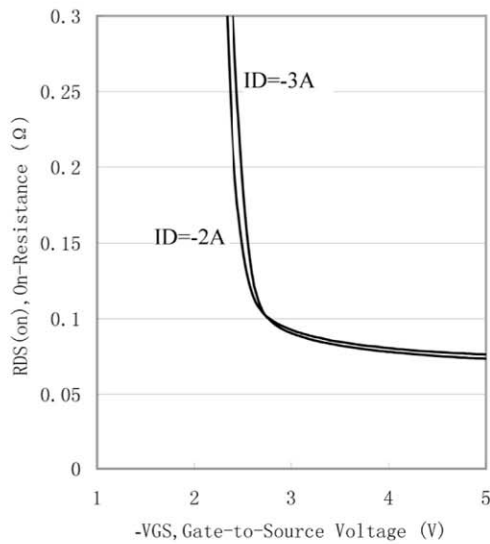


Figure 7. On-Resistance vs. Gate-to-Source Voltage

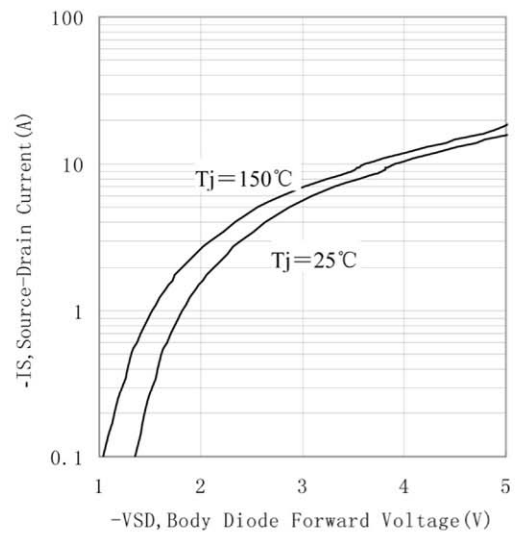


Figure 8. Source-Drain Diode Forward Voltage

Typical Characteristics

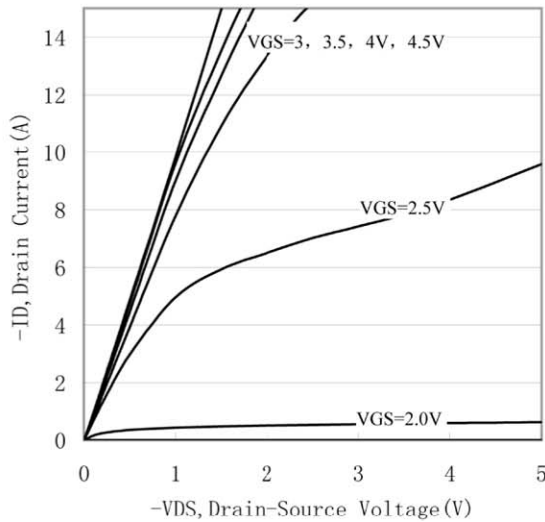


Figure 1. Output Characteristics

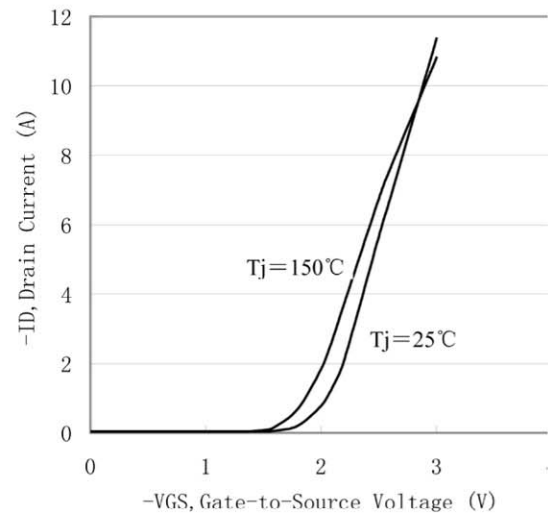


Figure 2. Transfer Characteristics

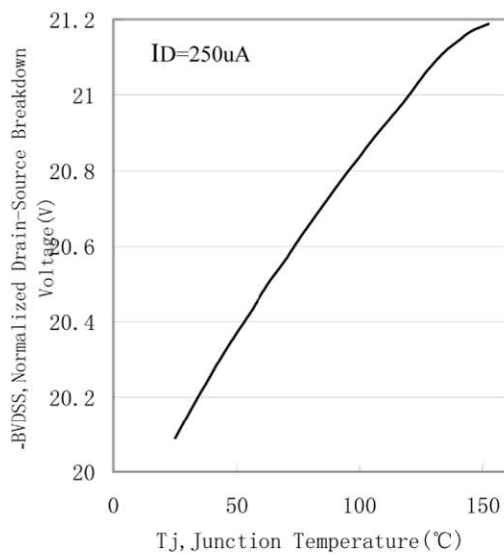


Figure 3. Breakdown Voltage Variation with Temperature

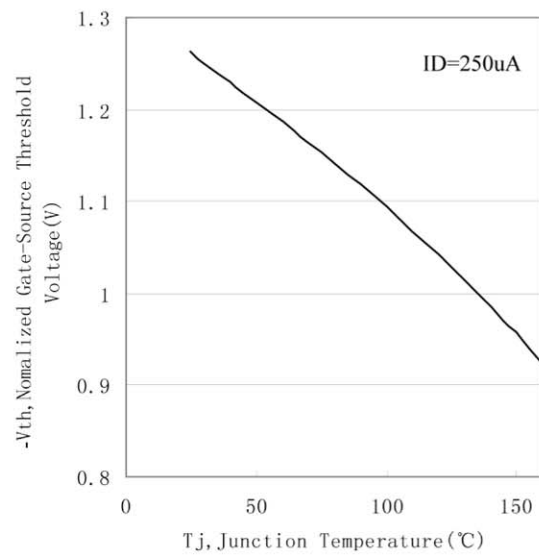


Figure 4. Gate Threshold Variation with Temperature